HDL-CR-047-2

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CR-047-2, Advanced Electro-Optical System Hardening--Phase II: Computer-Aided Susceptibility Analysis of the HOST Sensor Amplifier to IEMP, by John L. Gilbert

ADVANCED ELECTRO-OPTICAL SYSTEM HARDENING

Phase II: Computer-Aided Susceptibility Analysis of the HOST Sensor Amplifier to IEMP

December 1974

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Under Contract
DAAG39-73-C-0047

U.S. Army Materiel Command
HARRY DIAMOND LABORATORIES
Washington, D.C. 20438

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER HDL-CR-047-2	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE *(and Subtitle)* (U) Advanced Electro-Optical Systems Hardening Phase II - Computer-Aided Susceptibility Analysis of the HOST Sensor Amplifier to IEMP		5. TYPE OF REPORT & PERIOD COVERED Final Report 6. PERFORMING ORG. REPORT NUMBER 531W-01-CR
7. AUTHOR(s) John L. Gilbert		8. CONTRACT OR GRANT NUMBER(s) DAAG39-73-C-0047 HDL Proj: 358433
9. PERFORMING ORGANIZATION NAME AND ADDRESS General Research Corporation, Washington Operations, 7655 Old Springhouse Road, Westgate Research Park, McLean, Va. 22101		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Element Code: 6.23.06.A Washington Operations
11. CONTROLLING OFFICE NAME AND ADDRESS U. S. Army Materiel Command, Harry Diamond Laboratories, Washington, D.C. 20438		12. REPORT DATE December 1974 13. NUMBER OF PAGES 36
14. MONITORING AGENCY NAME & ADDRESS*(if different from Controlling Office)*		15. SECURITY CLASS. *(of this report)* Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

AMCMS Code: 632306.11.H7200
DA-1W362306AH72

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Electro-Optical Systems
Detectors

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This report supplied support to the Harry Diamond Laboratories on the effects of IEMP-induced transient pulses on the HOST detector amplifier. Computer simulation techniques were used to model the circuit's response to 1-μsec current pulses injected at the selected circuit locations. The most vulnerable subcircuit within the amplifier was found to be the detector bias power supply. Permanent damage was

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BLOCK 20: predicted to occur at the bias control input point for a cable response, resulting in the pickup of a 61-V, 0.064-A pulse, or greater.

CONTENTS

FIGURES

TABLES

SUMMARY

This study examines the vulnerability of one channel of the HOST detector amplifier to internal electromagnetic pulse (IEMP) induced transients coupling into the circuit at certain selected locations. Only the effects of the induced transients on the circuit, including transient-radiation effects on electronics (TREE) effects, are studied, not the IEMP coupling modes. The entry points for the transients are assumed to be cables interconnecting the various subcircuits composing the amplifier. The circuit operation was simulated using the NET-2 network analysis computer program. In the simulation, models were used which incorporated both linear and nonlinear operating characteristics. The induced transients were simulated using current pulses 1 μsec^2. HDL experimental component failure data for 1-μsec pulses were used for circuit component failure criteria.

The results of the analyses indicate that for the external field pickup points considered the amplifier circuit is most vulnerable to a pulse induced on the cable leading from the bias control switch to the input of the integrated circuit differential input driver composing part of the bias power supply circuitry (see Fig. 3). The critical induced pulse level found for the circuit was 61 V, 0.064 A for a positive-biased pulse, and -73 V, 0.39 A for a negative-biased pulse. With the inclusion of gamma radiation effects, the critical current level required for circuit failure is less certain, but may be up to a factor of 2 larger. The next most vulnerable subcircuit was the preamplifier. Three pulse entry points affecting the preamplifier were found to have approximately equal vulnerability, with damage occurring for 3-A pulses.

1 INTRODUCTION

The Ballistic Missile Defense Advance Technology Center (BMDATC) and the Army Material and Mechanics Research Center (AMMRC) are conducting a variety of programs designed to insure the operability of missile-borne electro-optical systems in a nuclear environment. As part of the overall effort, the Harry Diamond Laboratories (HDL) is performing an analytical and experimental study of the system-generated electromagnetic pulse (SGEMP) on major components of the HOST long-wave infrared (LWIR) sensor system. General Research Corporation (GRC) supplied support[1] to HDL on SGEMP and other problem areas.

A system located in a nuclear environment is exposed principally to gamma rays (prompt and delayed), electrons (prompt and delayed), x-rays, neutrons, and an electromagnetic pulse (EMP). The ionizing radiation can penetrate a system and produce transient-radiation effects in electronic (TREE) components. The EMP has a large magnitude and can affect a very large geographical area. Photoelectric and Compton effects within materials of a system produce free electrons which in turn produce electromagnetic fields giving rise to IEMP.

The IEMP environment within a HOST-like telescope assembly has been calculated previously.[1] It was found that the IEMP-generated fields could be of sufficient magnitude to damage circuit components. The damage was judged to occur as a result of IEMP-induced electrical pulses on cables interconnecting various subcircuits. IEMP interaction with individual component leads and within component cases, in addition to being extremely complex and difficult to predict, was estimated to be of secondary importance compared to cable pickup. Based on these earlier findings, this study attempts a detailed examination of the vulnerability of the HOST circuitry to electrical pulses induced by an IEMP environment.

The objective of this study is to determine analytically the injected pulse magnitude, such as might be induced by an IEMP environment, which will cause permanent component damage in the HOST sensor amplifier circuit. IEMP coupling into the circuit is modeled by injecting pulses at several selected circuit locations. Computed-aided modeling techniques are employed to simulate operation of subcircuits composing the amplifier and to monitor voltage and current signatures at susceptible active device terminals of each subcircuit during pulse injection. A critical pulse magnitude is determined for each injection point, which is the threshold signal level at the terminals of a particular device for failure. HDL experimental failure data for each device were used for circuit failure criteria.

[1] J. L. Gilbert et al., Advanced Electro-Optical System Hardening, EMP/IEMP, General Research Corp., CR-1-333, April 1974.

The approach used in the analysis was to model for each pulse entry point those components judged most susceptible to damage. Equivalent impedances were substituted in place of other components. To analytically determine the response of the circuitry to signals injected at the points of entry, computer-aided circuit modeling was performed using the NET-2 network analysis program.[1] NET-2 was chosen because of its flexibility and modeling accuracy in simulating circuit devices, and its ability to perform nonlinear transient radiation analysis. The program was used to simulate operation of those portions of the sensor amplifier circuit which were judged to be most susceptible to damage from large transient signals injected at each of the indicated points. Pulse injection simulation was accomplished by analytically connecting a pulsed current source to one of the injection points at a time, determining its effect on the circuit separate from effects due to injection at the other input points.

Models used for the components themselves included both linear and nonlinear features. Device models contained in the NET-2 programming, such as diodes and transistors, were used when possible. For integrated circuit components, terminal characteristics were modeled by using basic circuit devices such as resistors and dependent voltage sources. The characteristics for the components were derived from manufacturers' data. In general, the radiation characteristics for each of the integrated circuits were not known. Hence, general characteristics for each class of device were utilized. For this reason, the results given for the combined effects of EMP and a TREE environment (i.e., the simulated IEMP environment) are meant to indicate only the approximate characteristics the actual circuit might exhibit.

2 IEMP-CIRCUITRY INTERFACE

The circuit under investigation is the HOST single-channel amplifier. The HDL-supplied circuit diagram for the amplifier is shown in Fig. 1 (chart follows page 8). In the HOST system the focal plane electronics, preamplifier (drawing number 40362-516) and bias power supply (drawing number 40360-516) are located in the telescope, while the circumvention circuit (drawing number 40353-516), threshold detector circuit (drawing number 40368-516), and logarithmic amplifier (drawing number 40350-506) are located in the inner gimbal region. The amplifier circuit is composed of both discrete and integrated circuit components. The semiconductor components (those most likely to suffer damage in an IEMP environment) are listed in Table 1 along with a brief description of their location and circuit function.

[1] A. F. Malmberg, NET-2 Network Analysis Program - User's Manual, Harry Diamond Laboratories, September 1972.

The amplifier circuit is composed of five major subcircuits: the preamplifier (which includes the focal plane electronics), bias power supply, circumvention circuit; threshold detector circuit, and logarithmic amplifier. These subcircuits are shown in Figs. 2 through 6 respectively and have been redrawn from Fig. 1 for clarity and to include additional annotation. Circled numbers in the figures refer to circuit points in Fig. 1.

Interconnecting cables judged susceptible to IEMP pickup are used between the focal plane electronics and the preamplifier and bias power supply, between the telescope and inner gimbal subcircuits, and at the logarithmic amplifier output. Examination of these cable connection points has led to a determination by GRC and HDL personnel of IEMP entry points into the circuit. The results of this analysis, then, are only applicable to IEMP pickup at these points. For reference and for identification purposes in the circuit diagrams, a number is assigned to each of these induced pulse entry points, which are defined as follows:

(1) Lead connecting the MOSFET source terminal to the preamplifier input (Fig. 2).

(2) Lead connecting the sensor to the bias power supply (Figs. 2 and 3).

(3) Lead from the bias control switch to the bias power supply (Fig. 3).

(4) Lead connecting the preamplifier output stage to the negative input point of the circumvention circuit (Figs. 2 and 4).

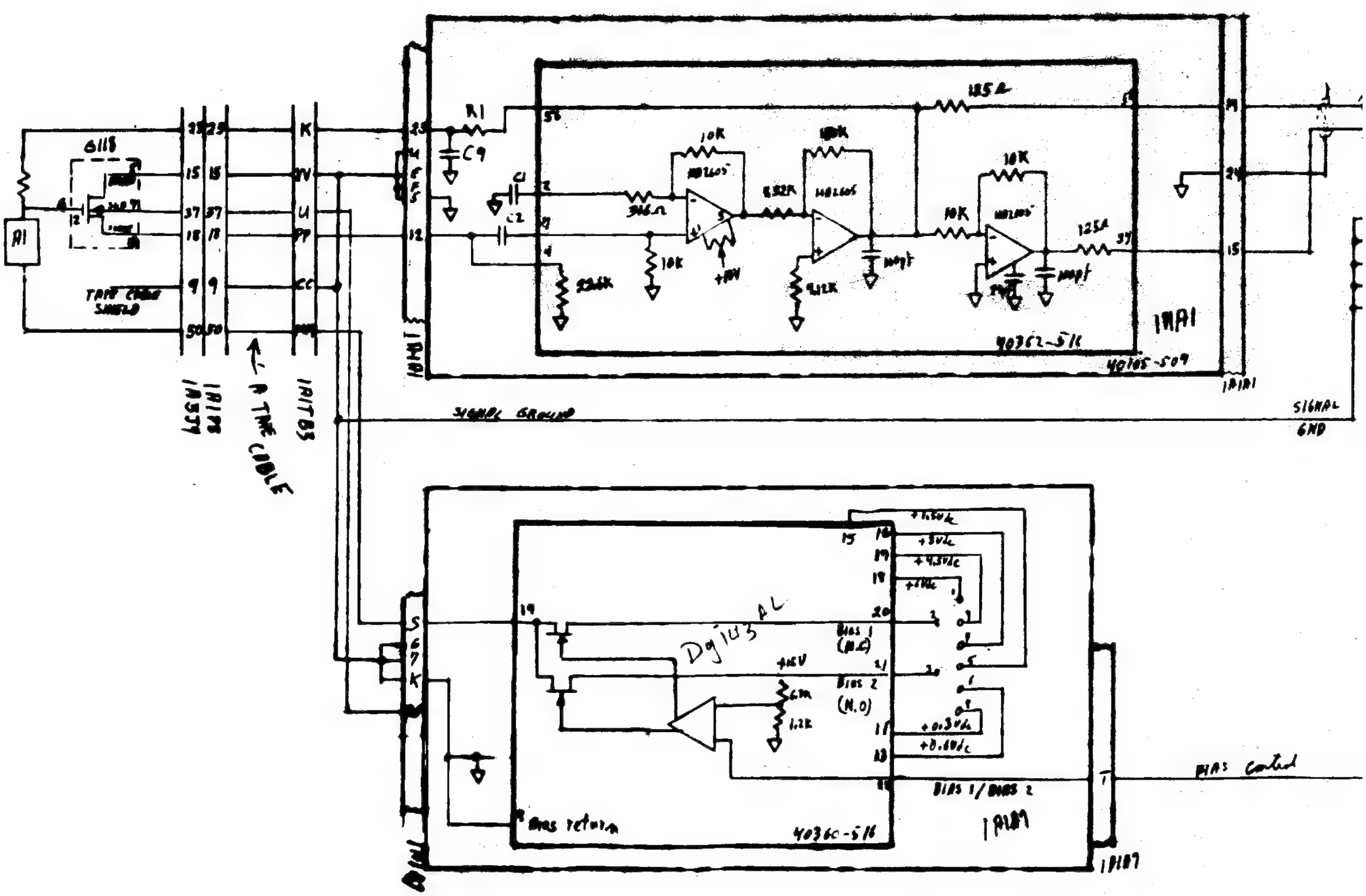
(5) Lead connecting the preamplifier/sensor feedback path to the positive input point of the circumvention circuit (Figs. 2 and 4).

(6) HOST sensor circuit output terminal, which connects to the logarithmic amplifier output and to the threshold detector circuit (Figs. 5 and 6).

3 CIRCUIT ANALYSIS

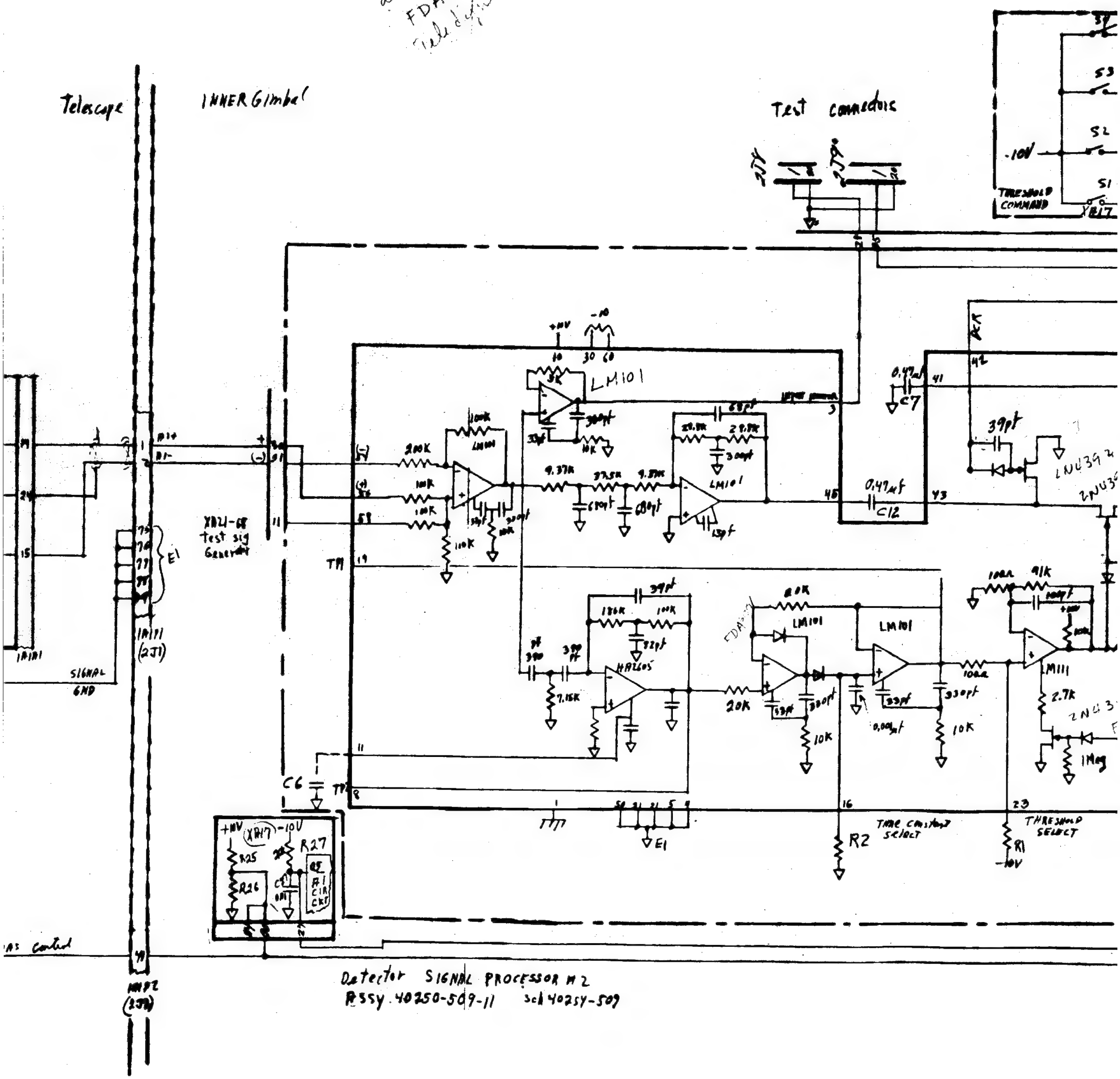
To find the critical pulse magnitudes for each pulse entry point, an analysis was performed to determine the circuit response to an injected square current pulse of 1-μsec duration. This pulse shape permits the application of the HDL device damage-level experimental results which indicate the vulnerability of each individual circuit component to a

Telescope

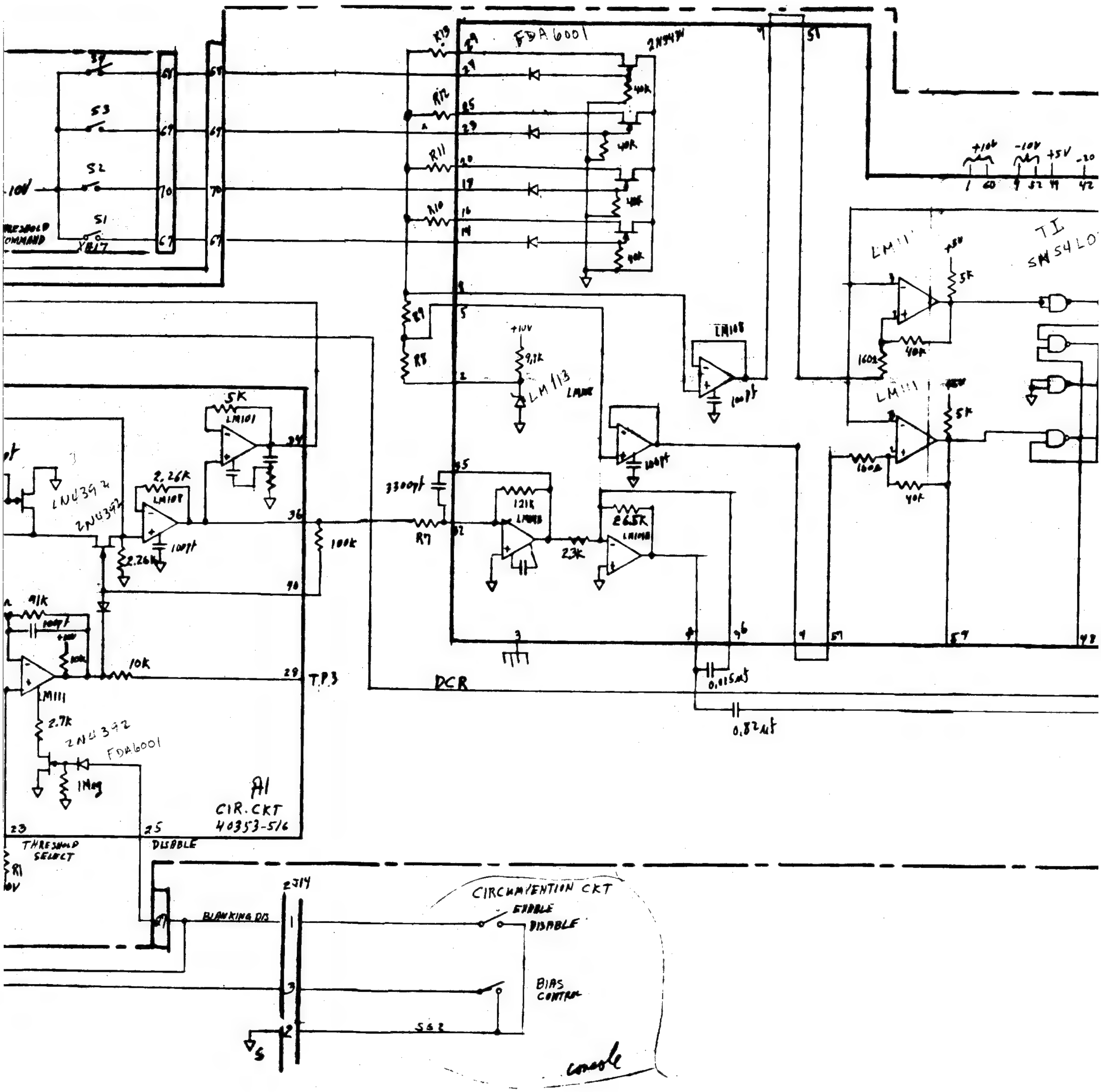


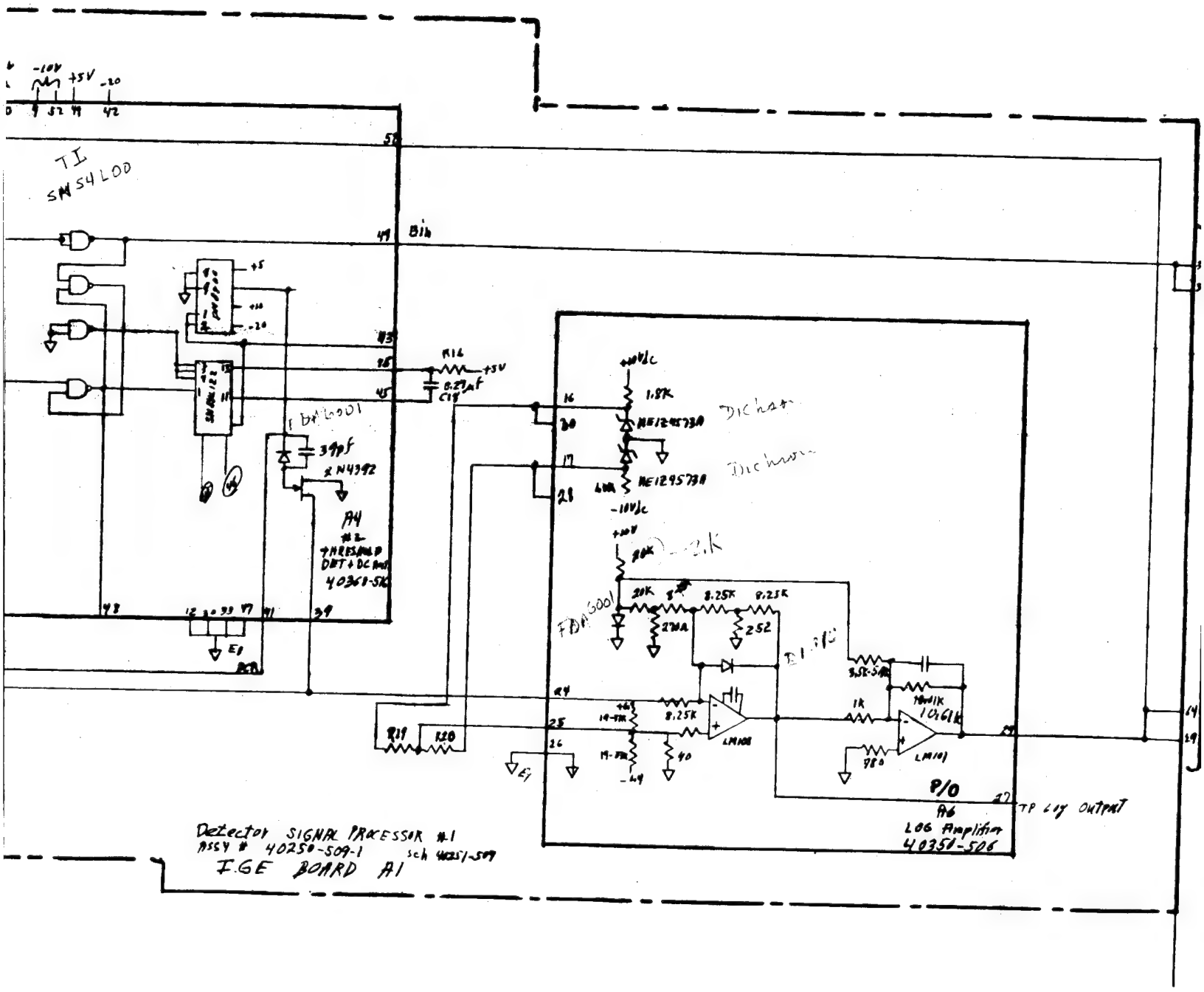
R1
C9
10K
125Ω
TAPE CABLE SHIELD
SIGNAL GROUND
SIGNAL GND
1A1A1
40362-516
40105-509
Dg143 AL
BIAS 1 (N.C)
BIAS 2 (N.O)
Bias return
40360-516
BIAS 1 / BIAS 2
Bias Control

all diodes not listed
FDA6001
Teledyne

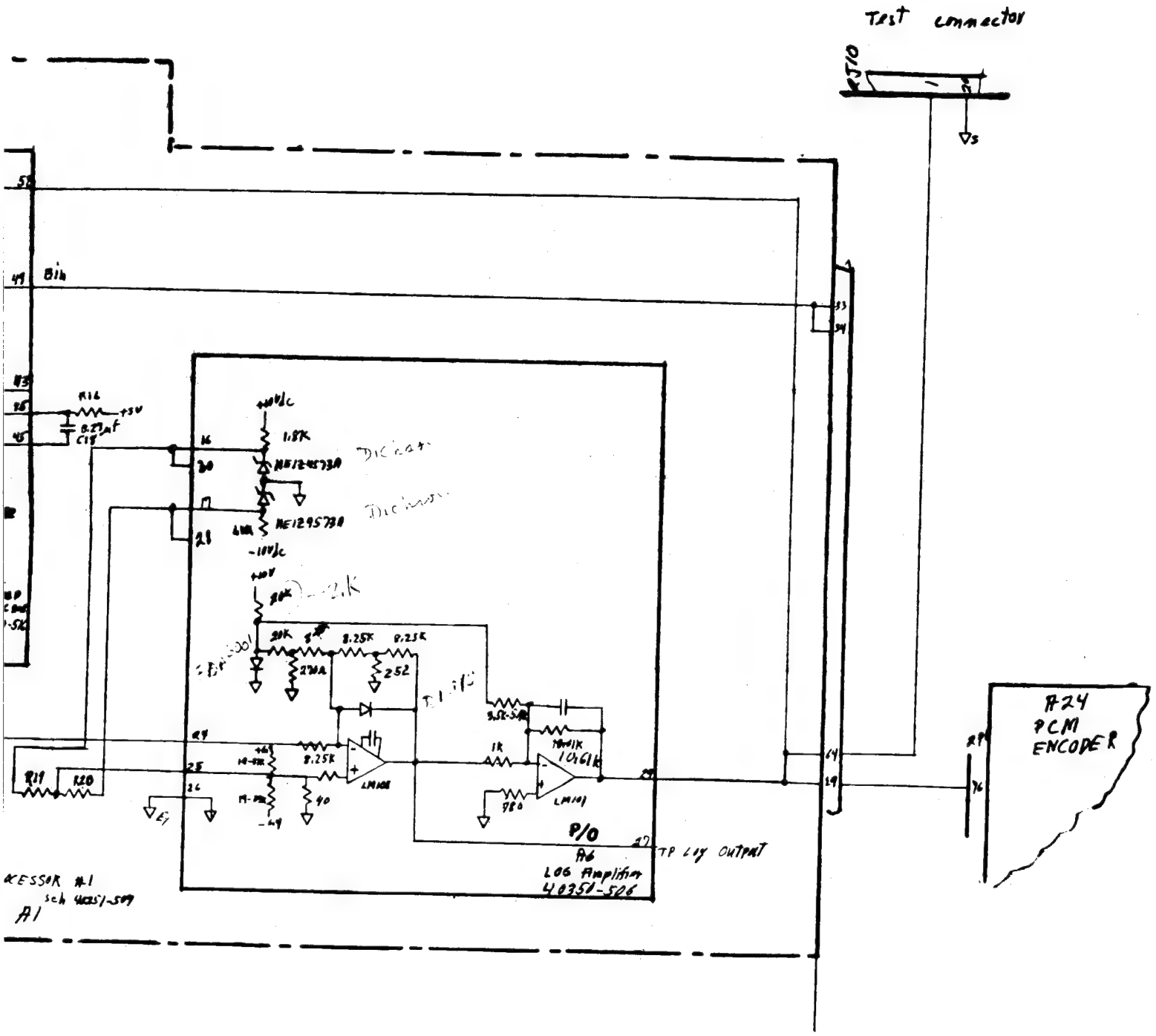


Detector SIGNAL PROCESSOR #2
Assy 40250-509-11 sch 40254-509


FDA6001
LM108
LM111
LM101
LM113
TI SN54LO
S1
S2
S3
THRESHOLD COMMAND
THRESHOLD SELECT
DISABLE
BLANKING DIS
T.P.3
DCR
0.015uf
0.82uf
3300pf
100pf
A1
CIR. CKT
40353-5/6
CIRCUMVENTION CKT
ENABLE
DISABLE
BIAS CONTROL
console
+10V
-10V
+5V



Detector SIGNAL PROCESSOR #1
ASSY # 40250-509-1 sch 40251-509
I.F.E BOARD A1



Single channel Amp

9-4-73 W.C. Mark

TABLE 1

HOST SEMICONDUCTOR COMPONENTS

DEVICE	DESCRIPTION	LOCATION	CIRCUIT FUNCTION	MANUFACTURER
G118AL	MOSFET	TELESCOPE		SILICONIX
HA2605	OP-AMP	TELESCOPE	PREAMPLIFIER DETECTOR BIAS SUPPLY DETECTOR SIGNAL PROCESSOR #2	HARRIS
DG143AI	DIFFERENTIAL INPUT DRIVER	TELESCOPE	DETECTOR BIAS SUPPLY	SILICONIX
2N2484	LOW POWER TRANSISTOR	TELESCOPE	DETECTOR BIAS SUPPLY	SOLID STATE DEVICES
2N2605	LOW POWER TRANSISTOR	TELESCOPE	DETECTOR BIAS	SOLID STATE DEVICES
1N821	REFERENCE DIODE	TELESCOPE	DETECTOR BIAS SUPPLY	DICKSON
LM101F	OP-AMP	INNER GIMBAL	DETECTOR SIGNAL PROCESSOR #2	NATIONAL SEMICONDUCTOR

TABLE 1

HOST SEMICONDUCTOR COMPONENTS (Cont.)

DEVICE	DESCRIPTION	LOCATION	CIRCUIT FUNCTION	MANUFACTURER
LM108F	OP-AMP	INNER GIMBAL	DETECTOR SIGNAL PROCESSOR #2 THRESHOLD DET. & D.C. RESTORER	NATIONAL SEMICONDUCTOR
LM111F	VOLTAGE COMPARATOR	INNER GIMBAL	DETECTOR SIGNAL PROCESSOR #2	NATIONAL SEMICONDUCTOR
2N4392	N CHANNEL JFET	INNER GIMBAL	DETECTOR SIGNAL PROCESSOR #2 DETECTOR SIGNAL PROCESSOR #2	SOLITRON DEVICES
FDA60001* (1N914)	SWITCHING DIODE	INNER GIMBAL	DETECTOR SIGNAL PROCESSOR #1 THRESHOLD DET. & D.C. RESTORER	FAIRCHILD
LM113H	REFERENCE DIODE	INNEP IMBAL	THRESHOLD DET. & D.C. RESTORER	NATIONAL SEMICONDUCTOR
LM101AF	OP-AMP	INNER GIMBAI	THRESHOLD DET. & D.C. RESTORER	NATIONAL SEMICONDUCTOR

TABLE 1

HOST SEMICONDUCTOR COMPONENTS (Cont.)

DEVICE	DESCRIPTION	LOCATION	CIRCUIT FUNCTION	MANUFACTURER
SN54L00	LOW POWER TTL GATE	INNER GIMBAL	THRESHOLD DET. & D.C. RESTORER	TEXAS INSTRUMENTS
DM8800	GATE DRIVER	INNER GIMBAL	THRESHOLD DET & D.C. RESTORER	NATIONAL SEMICONDUCTOR
SN54L122	MULTIVIBRATOR	INNER GIMBAL	THRESHOLD DET. & D.C. RESTORER	TEXAS INSTRUMENTS
2N543*	N CHANNEL JFET	INNER GIMBAL	THRESHOLD DET. & D.C. RESTORER	SILICONIX
D1914	REFERENCE DIODE	INNER GIMBAL	LOG AMPLIFIER	DICKSON
ME1Z4573A	REFERENCE DIODE	INNER GIMBAL	LOG AMPLIFIER	DICKSON

* RECOMMENDED SUBSTITUTION BY AUTONETICS

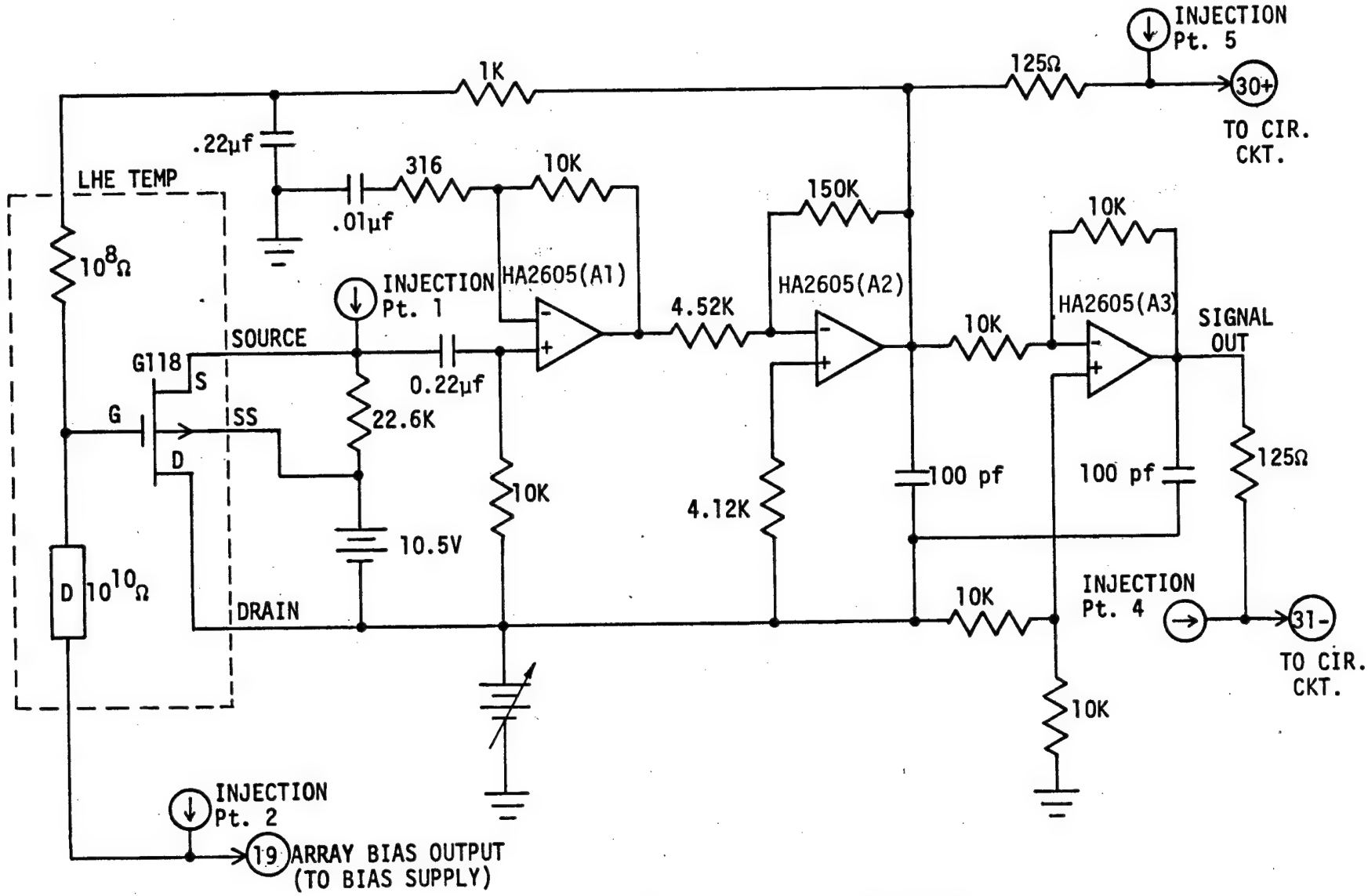


Figure 2. HOST Preamplifier Subcircuit (40362-516)

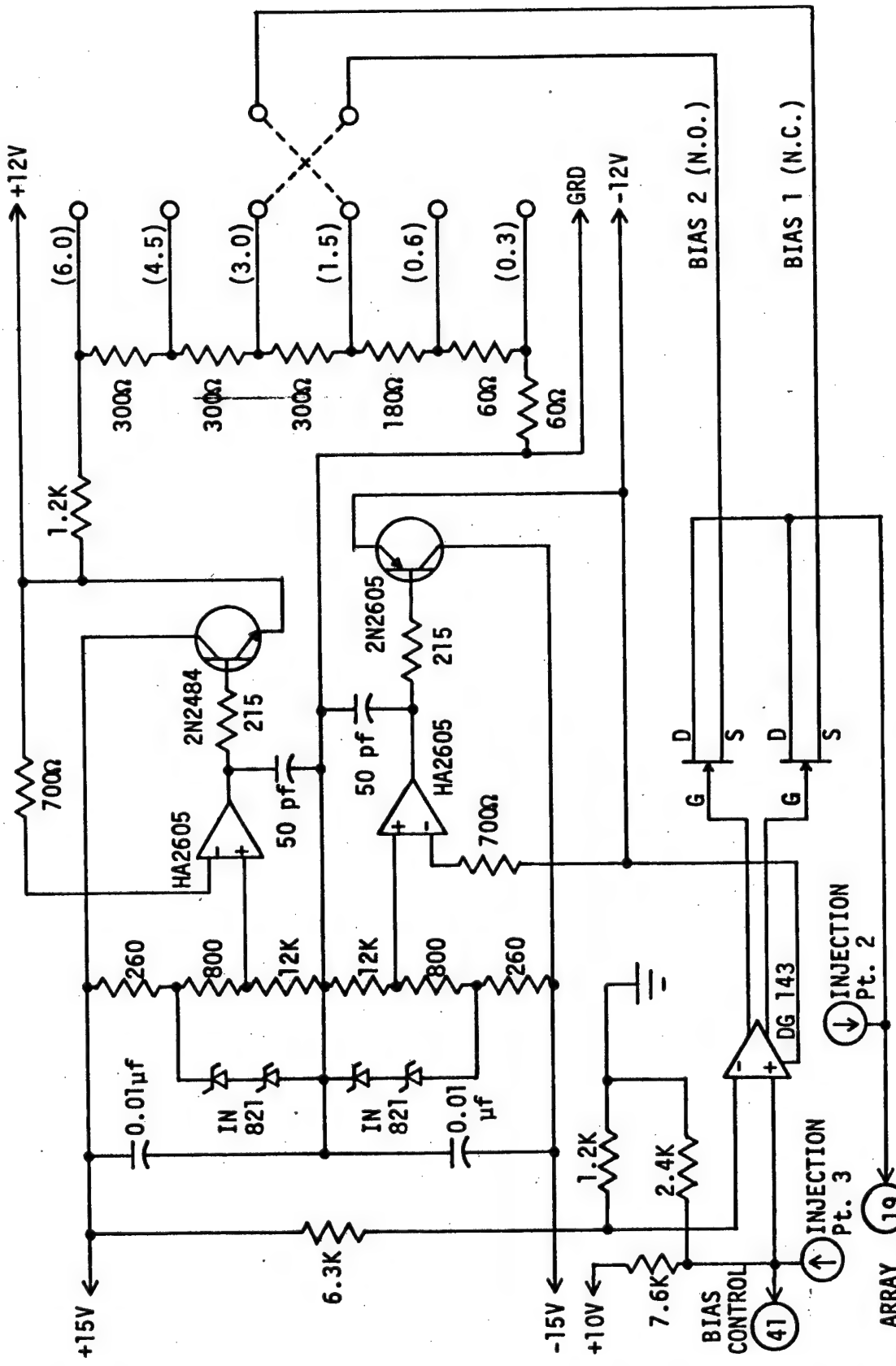


Figure 3. HOST Bias Power Supply Subcircuit (40360-516)

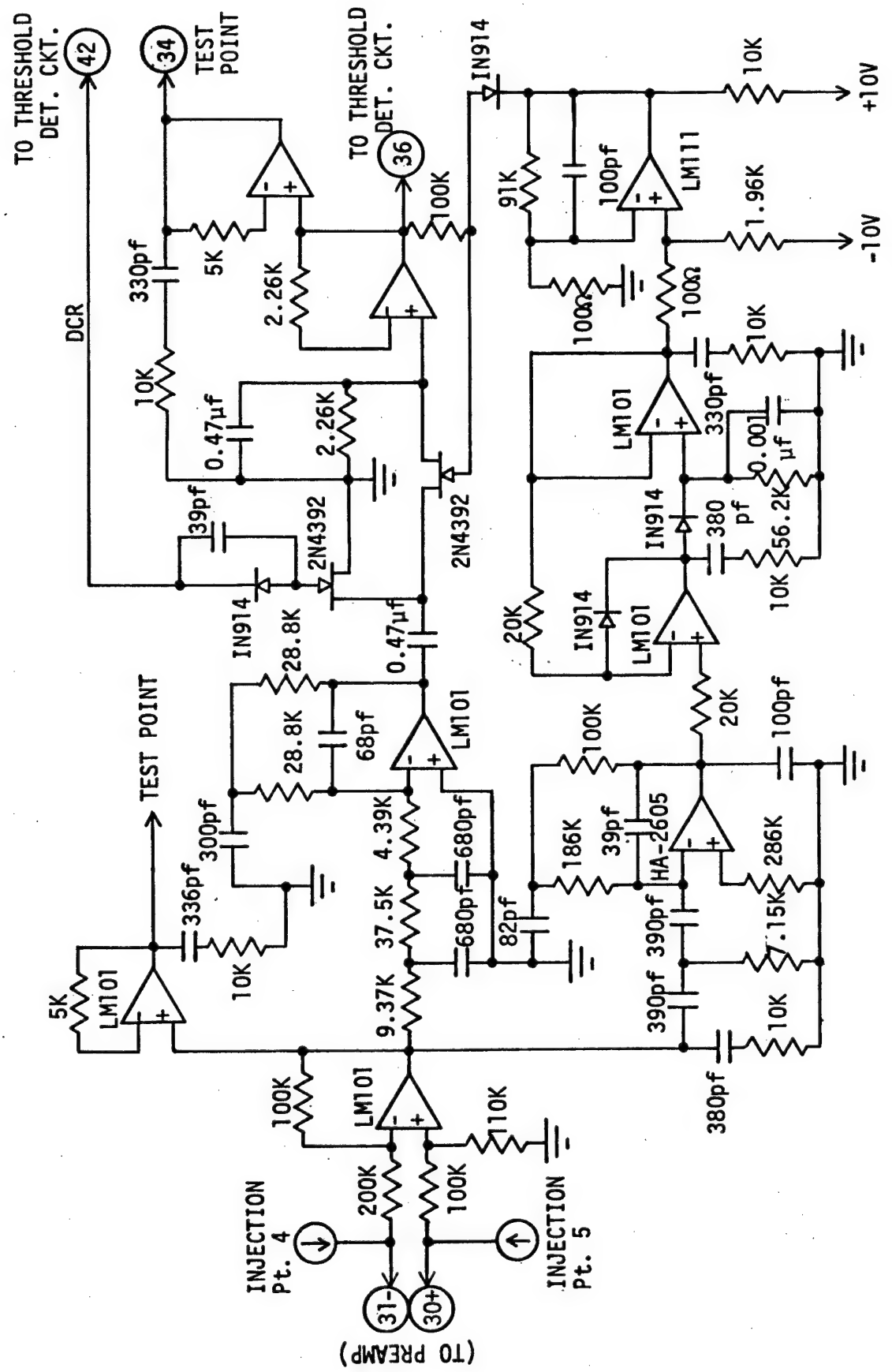


Figure 4. HOST Circumvention Subcircuit (40353-516)

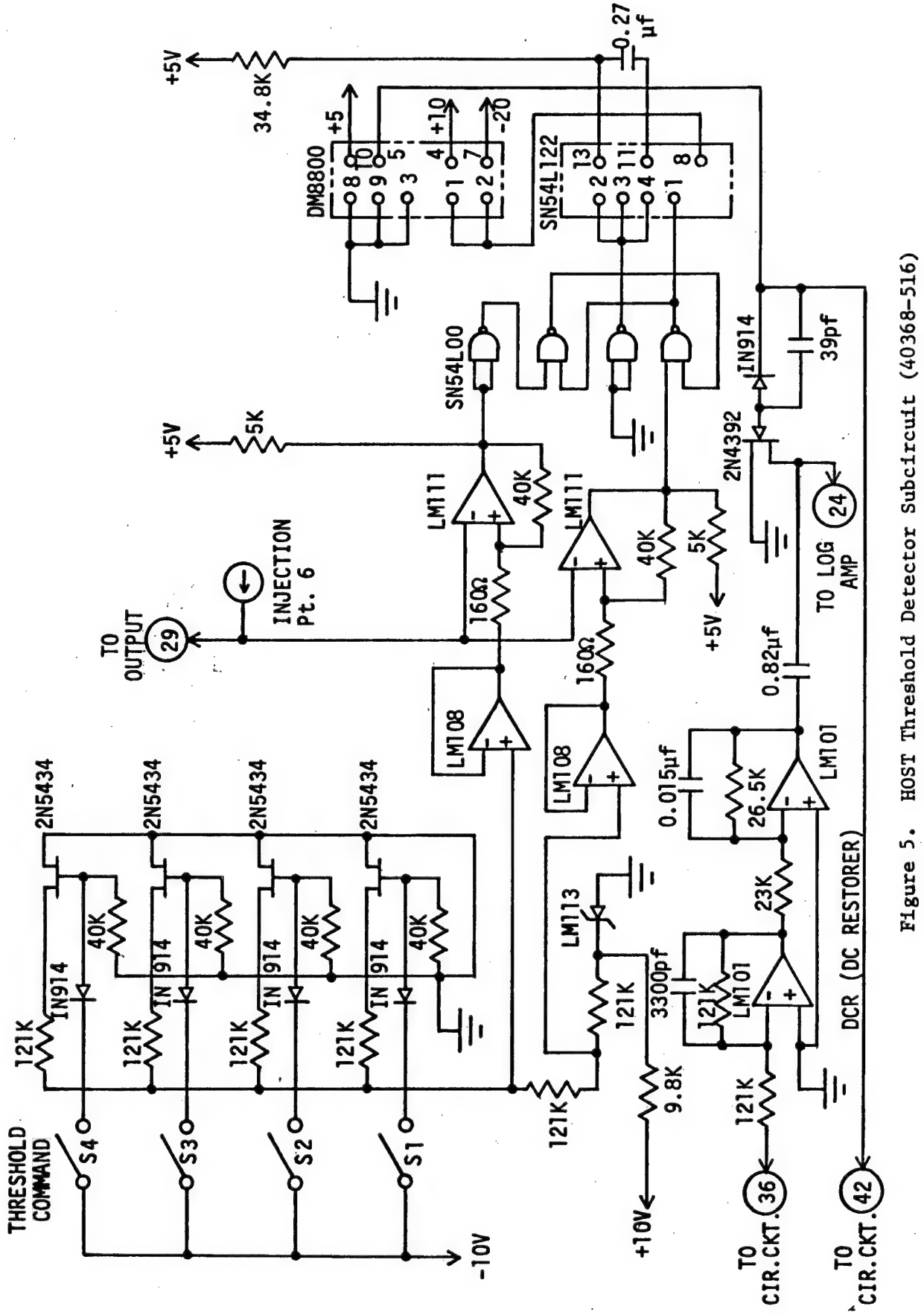


Figure 5. HOST Threshold Detector Subcircuit (40368-516)

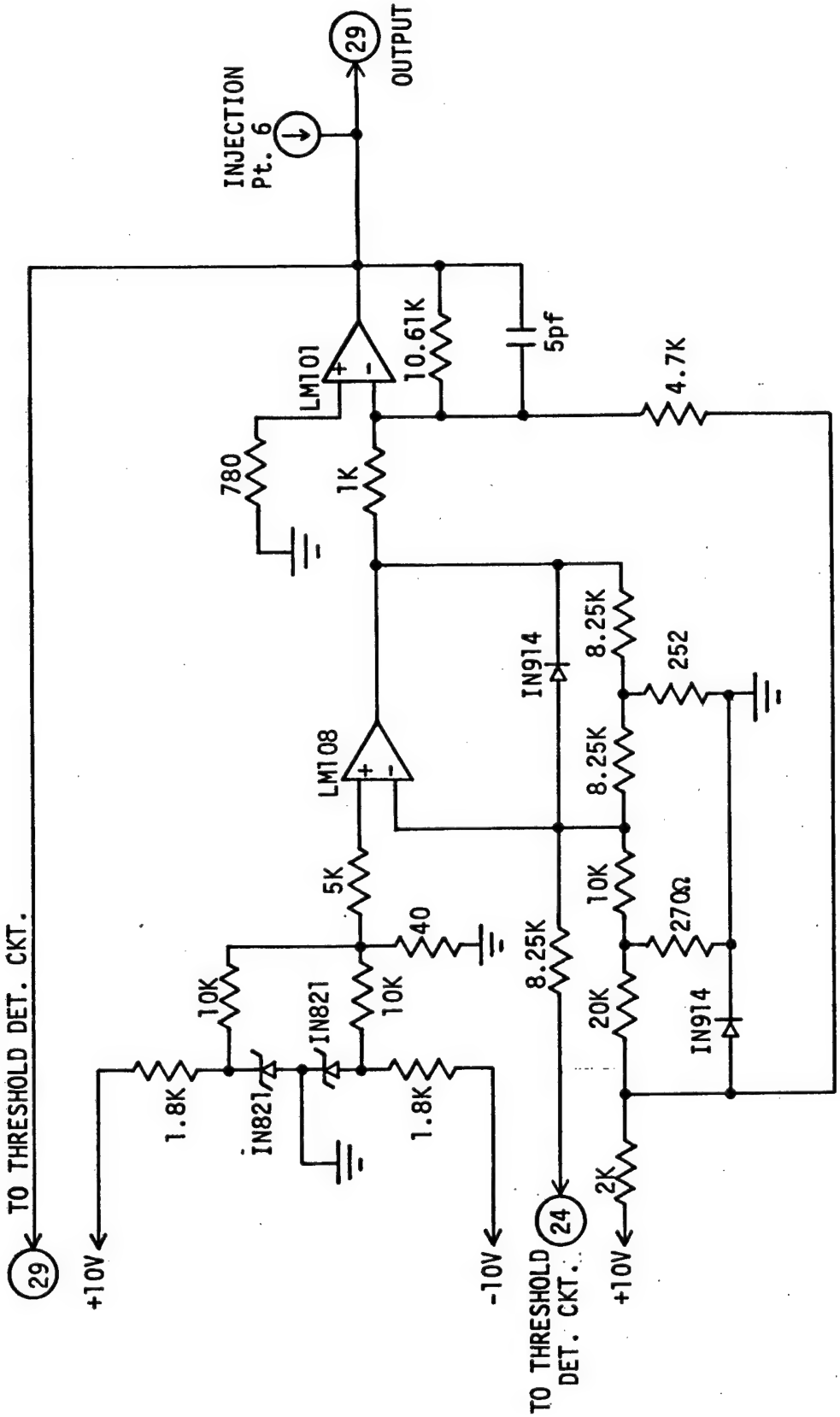


Figure 6. HOST Logarithmic Amplifier Subcircuit (40350-506)

1-μsec current pulse.[1] These experimental results are shown in Table 2, and are used in this study as device damage criteria (referred to as the critical pulse level). The double entries shown in the table indicate first the peak value reached, and second the steady-state value. For each pulse injection point, the critical pulse level is reached when the current at any of the susceptible device terminals reaches or exceeds the current shown in Table 2 for the terminal of the specific component.

3.1 COMPONENT MODELING

Modeling of the circuit devices was accomplished by utilizing the NET-2 supplied device models when possible or by creating models from the basic circuit elements available in NET-2 (resistors, capacitors, dependent voltage sources, etc.). The NET-2 supplied device models are linear; most of them have provision for the inclusion of radiation effects. The NET-2 models utilized in the analysis included those for the junction diode, zener diode, junction field-effect transistor (JFET) and metal oxide semiconductor field-effect transistor (MOSFET). In general, the models for these devices are based on dependent current sources in conjunction with resistors and capacitors to model the active and saturation operating regions, but not the breakdown region. The junction diode model is of the Ebers-Moll type and exhibits normal forward conduction, reverse cutoff behavior and storage time effects. The model does not include junction breakdown at large reverse voltage or conductivity modulation of the base region. The zener diode model included the same features as the junction diode model and also included zener breakdown behavior. The MOSFET model exhibits the very high gate input impedance normally found, may represent either PNP or NPN structure, and may be operated in both the enhancement and depletion modes. Symmetric characteristics with respect to drain-source voltage polarity is obtained with the model. The JFET model may represent either PNP or NPN structure and asymmetric characteristics are available with respect to drain-source voltage polarity. In each of the models, current sources to model radiation effects are included automatically whenever a neutron or gamma radiation source is specified. (In this analysis only gamma radiation effects are considered.) Breakdown characteristics for the FET models were added externally by using zener diode models incorporating appropriate breakdown voltage and bulk resistance parameters derived from the manufacturers specifications.

Most of the amplifier circuit operation depends upon the use of integrated circuit (IC) operational amplifiers. The model used to

[1] W. L. Vault and L. Harper, Advanced Electro-Optical System Hardening Study; Phase I-EMP/IEMP Susceptibility of HOST Sensor Electronic Components, Final Report for Period 1 July 1973 - 31 July 1974, to be published.

TABLE 2

EXPERIMENTAL COMPONENT DAMAGE CRITERIA (CRITICAL VOLTAGES, CURRENTS AND ABSORBED ENERGIES)

Device	Simulated Test	Terminal Pair	Pulse Bias	Voltage (V)	Current (A)	Energy (μJ)
1N3066	EP[a]	C - A	+	187	18.6	1576
			−	100.5 ± 2.5	1.27 ± .03	90 ± 7
1N914	EP	C - A	+	19.3 ± 0.1	20.3 ± 1.2	176.5 ± 21.5
			−	110.6 ± 6.8	1.9 ± 0.6	98.8 ± 15.0
1N821	EP	C - A	+	80	36	No Failure
			−	30	40	No Failure
LM113	EP	C - A	+	256±11, 109.6±11	27.6±2.5, 13.1±1.4	461 ± 99.5
			−	135±2.8, 126.3±6.5	21.3±0.9, 9.3±2.1	297.3 ± 53.7
2N2484	CE[b]	E - B	+	106.3±54.9, 41.3±15	17.8±3.1, 17±3.2	647.8 ± 423
			−	36.6±6.6, 33.6±6.6	2.8 ± 4, 2.48 ± .3	72.6 ± 6.9
	CE	C - B	+			
			−	160, 40	13, 12	1882
	EP	C - B	+	62.5±2.5, 20.5±2.5	22, 21	441.9 ± 53.9
			−	754 ±258, 221±86.4	14.1±4.5, 11.9±5.0	450±347
2N2605	EP	E - B	+	28, 22	16, 15.8	439
			−	42, 24	2.8, 2.5	32
	CE	E - B	+	56, 25.7 ± .47	16, 14.7 ± .47	388.7 ± 4.7
			−	35.3±3.4, 31.3±1.9	1.6 ± .05	56.6 ± 7.1

a - EP is for EMP Simulated Environments

b - CE is for combined TREE and EMP Simulated Environments

TABLE 2

EXPERIMENTAL COMPONENT DAMAGE CRITERIA (CRITICAL VOLTAGES, CURRENTS AND ABSORBED ENERGIES) (Cont.)

Device	Simulated Test	Terminal Pair	Pulse Bias	Voltage (V)	Current (A)	Energy (μJ)
	EP	C - B	+	60, 13	19.8	251
			-	143, 100	3.2, 1.7	125
	CE	C - B	+	33.7 ± .47, 7.0	20, 19.5	659.6 ± 9.1
			-	96.7±23.2, 77.3±32	2.6±0.7, 1.8±0.8	67.2 ± 4.8
G118	EP	G1-G2	+	108±53.7, 53±26	1.05±0.75, 2.05±0.07	100.7 ± 40.4
			-	119.7, 28.4	0.86, 2.57	74.6
	CE	G1-G2	+	105.5±40.5, 31.5±8.6	7.8 ±1.5,	179
			-	156, 80.4	0.8, 2.87	177
	EP	G4 - D	+	78.9, 43.8	2.9,	116
2N4392	EP	G - D, S	+	26.7±.88, 14.1±2.07	11.8 ± 3.2,	164.9 ± 59
			-	92 ± 8, 41	4.38 ± .28	266 ± 89
	CE	G - D, S	+	23.5±.2,15.4±.1	15.6±.5	232.3±11.7
			-	102.4±2.4, 86.7±15	5.7 ± .4, 5.15±.35	321.2 ± 68.6
	EP	G - S	+	26, 14.5 ± .5	12.1 ± .9	184 ± 18
			-	92 ± 4.9, 14	12.1 ± .9	184 ± 18
	CE	G - S	+	50.4±17.6, 25.4±9.3	14.3±2.6, 14.8±1.8	205.4 ± 87
			-	90.9±5.9, 67.8±12.6	4.23±.48, 3.7±.36	172.6 ± 59
2N5434	EP	G - D,S	+	28.1, 14.8	28.8,	459
			-	130	5.6	543
	CE	G - D,S	+			
			-	82±4.3, 71.4±12	5.93±.13, 6.19±.39	358±80

TABLE 2

EXPERIMENTAL COMPONENT DAMAGE CRITERIA (CRITICAL VOLTAGES, CURRENTS AND ABSORBED ENERGIES) (Cont.)

Device	Simulated Test	Terminal Pair	Pulse Bias	Voltage (V)	Current (A)	Energy (μJ)
	EP	G - S	+	30.7±6.5, 12±2.5	10.6±3.	137.3±54.4
			-	75.4±5.4, 70.5±0.5	3.18 ± 0.48	218 ± 29
	CE	G - S	+	24±2, 12.9±0.9	15.2±0.6, 16.2±1.6	212±33
			-	92.5±7.5, 73 ± 31	495±0.25, 5.45±.45	385±29
HA2605	EP	In^+-In^-	+	91.5 ± 2.5	3.99 ± 0.12	243 ± 8.5
			-	149 ± 10	2.15 ± 1.4	202.5 ± 74.5
	CE	In^+-In^-	+	93, 82	5.5	256
			-	95	5.24	345
	EP	Out-In^+	+	170 ± 4, 124 ± 1	3.03 ± 0.35	328
			-	126 ± 6.5,	3.02 + 0.5	288 ± 85
	CE	Out-In^+	+	209, 154	5.03	566
			-	162, 119	5.97	696
LM108	EP	In^+-In^-	+	44.7, 32.2	4.15, 3.82	113
			-	42.6, 30.2	4.8, 4.54	94.5
	CE	In^+-In^-	+	27±2.4, 20.4±3.7	4.04±0.27, 3.9±0.18	67.2 ± 18.8
			-	68.2, 43.7	4.43, 3.9	120
	EP	Out-In^+	+	259, 207	4.65, 4.44	716
			-	248, 146	4.97, 4.52	736
	CE	Out-In^+	+	201, 153	4.9, 4.5	613
			-	177, 140	4.62, 4.00	540

TABLE 2

EXPERIMENTAL COMPONENT DAMAGE CRITERIA (CRITICAL VOLTAGES, CURRENTS AND ABSORBED ENERGIES) (Cont.)

Device	Simulated Test	Terminal Pair	Pulse Bias	Voltage (V)	Current (A)	Energy (μJ)
LM101	EP	In^+-In^-	+	44.7, 32.2	4.2, 3.82	94.5
			−	42.6, 30.2	4.8, 4.54	113
	CE	In^+-In^-	+	27.2 ± 6.7, 14,8	3.87 ± 1.9	69.3 ± 19.3
			−	68.2, 43.7	4.4, 3.9	120
	EP	Out-In^+	+	259, 207	4.7, 4.44	716
			−	248, 146	4.97, 4.52	736
	CE	Out-In^+	+	201, 153	4.9, 4.45	613
			−	177, 140	4.62, 4.01	540
DG 143	EP	In-V_{EE}	+	68.5 ± 15.5	3.0 ± 0.8	77.5 ± 21.5
			−	37 ± 4	1.73 ± 0.02	26.7 ± 0.4
	EP	In-V_{EE}[c]	+	52.8	0.034	1.3
			−	43.6	.346	10.9
	EP	S-D	+	18, 32	3.8, 3.4	29.9
			−	20. 42	4.2, 4	26.9
	CE	In-In[d]	+		Data Not Supplied	
			−			
DM8800	EP	In-Gr	+	72, 28	1.73	49.9
			−	169, 71	2.8	197.6
	CE	In-Gr	+	32.7, 15.3	4.86	54
			−	151, 105	2.65, 1.99	239
	EP	Out-Gr	+	120	5	180
			−	152	3.6	80

c - Circuit was actively biased

d - 100 ns electrical pulse

TABLE 2

EXPERIMENTAL COMPONENT DAMAGE CRITERIA (CRITICAL VOLTAGES, CURRENTS AND ABSORBED ENERGIES((Cont.)

Device	Simulated Test	Terminal Pair	Pulse Bias	Voltage (V)	Current (A)	Energy (μJ)
SN54L00	EP	In-Gr.	+	60.6 ± 5.3, 47.5±8.3	1.59±0.33[4], 1.925±0.36	30 ± 8.2
			−	76.3±17.3,50.6±19.1	3.06±0.59, 3.45±0.51	184.6 ± 48.8
	CE	In-Gr.	+	63±7.8, 29.5±6.1	2.38±0.37, 3.58±.83	103.56 ± 28.77
			−	278 ± 116, 148.8±73.4	3.2 ± 0.2, 4.8±0.61	211.06 ± 40.05
	EP	Out-Gr.	+	28.3±4.7, 16.7±2.4	5.3±0.47, 5.8±0.85	87 ± 25.8
			−	32.3 ± 23.9,	2.57 ± 0.74	62.6 ± 38
	CE	Out-Gr.	+	88.3±2.4, 71.7±6.2	3.5, 5.1 ± 0.3	141.3
			−	40,	2.9±0.08,3.5±.34	78.1 ± 29.4
SN54L122	EP	In-Gr.	+	53.3 ± 12.28	3.36 ± 1.31	185 ± 86.9
			−	44.5 ± 6.5	.612 ± 0.07	16.8 ± 8
	CE	In-Gr	+	42	2.16	64
			−	44.8	2.25	77.9
	EP	Out-Gr	+	34.33 ± 8.73	3.1 ± 1.21	54.7 ± 6.8
			−	26.5 ± 0.5	7.85 ± 0.65	241.7 ± 82.1
	CE	Out-G4	+	38.4	2.59	55
			−	26.8 ± 4.2	5.54 ± 0.44	117.5 ± 13.5

simulate operational amplifiers was of the type described by Nichols[1] for characterizing an amplifier's unit step response and included the radiation response and the nonlinear effect of output voltage limiting. This model had the advantage of being simple while still adequately modeling the linear operating region and allowing nonlinear effects to be easily incorporated. For instance, one nonlinear effect included in the model was voltage limiting which occurred when the input stage saturated. For worst case modeling of this effect, the output voltage level of the model reached and remained at the power supply voltage level. In general, however, the nonlinear characteristics for the specific devices used in the circuit (both preceding and during failure) were not known. Therefore, the approach (particularly for IC's) was to model possible current paths within the devices during failure and assign breakdown voltages and resistances for these current paths on the basis of information available from manufacturers' data sheets. These current paths for the operational amplifiers were between input terminals, input and output terminals, or between either input or output terminals and ground. The IC power supply was assumed to represent a low resistance path to ground for the pulse length used. The paths were modeled using zener diodes, while the actual paths depend on the particular circuit location of each device. The general rule applied was to assign a breakdown voltage equal to twice the manufacturer's absolute maximum rating for the terminals in question. The resistance for the current paths, chosen by analyzing each particular IC's equivalent circuit, was determined by assigning a constant value of 5 Ω to each forward-biased junction (as determined by the current pulse polarity) encountered along the path, and by assigning a value of 15 Ω to each back-biased junction. This method was used for each operational amplifier modeled. The reasoning behind this approach was that in the absence of actual failure characteristics, adequate modeling of the behavior of each device should be accomplished in a way which was as simple and as general as possible.

Modeling of other integrated circuit components in general involved modification of the operational amplifier model. The DG143 differential input driver was represented using the operational amplifier model as the input stage which controlled the gate terminals of two NET-2 JFET models acting as switches. The SN54L00 digital TTL gate and the LM111 voltage comparator were represented by modifying the operational amplifier model to account for their digital output characteristics. Other operational amplifier model features, such as output voltage limiting and zener diodes to model the current paths during failure, were retained. Since the approach for modeling the circuit operation (described in Sec. 3.2) involved modeling in detail only those components most susceptible to damage, models were not developed for IC devices such as the DM8800 gate driver and the SN54L122 monostable multivibrator.

[1] J. S. Nichols et al., "Characterization and Modeling of the 709 Integrated Circuit Operational Amplifier in an Ionizing Radiation Environment," IEEE Trans. on Nuclear Science, NS-16, No. 6, December 1969.

3.2 CIRCUIT MODELING

For each pulse injection point an analysis was made to determine the components most likely to suffer damage. In addition, it was determined whether, as a result of being perturbed by the injected pulse, any given device could supply enough energy to the next device to damage it. In most cases, only those components closest to the pulse injection point were judged susceptible to damage. This judgment was based on the following predictions: (1) most of the pulse energy would be dissipated along the lowest resistance path to ground, (2) this path normally would involve only one component, (3) none of the components could be driven hard enough to produce large secondary pulses capable of damaging other components, and (4) devices such as discrete resistors and capacitors would be immune to damage. The third prediction is based mainly on the limitation imposed by each component's power supply (i.e., limited power available and they provide a low resistance path to ground). Based on these predictions the circuit analysis for each injection point included detailed modeling of only those components judged susceptible to damage. Other components in the circuit were replaced by equivalent impedances which included appropriate radiation effects characteristics. For the inclusion of radiation effects in the computer simulations, a gamma dot source of 10^{10} rad (Si)/sec was used. In addition the effects of gamma radiation are implicitly included in the approach used. For the analysis of any particular injection point, the magnitude of the injected current pulse is increased until a critical pulse level is reached as determined from the experimental data of Table 2. Hence, the values specified in Table 2 control to a certain extent the radiation response characteristics near failure of each of the components.

Figure 7 illustrates the circuit modeling performed for injection point one. Detailed component models were used for only the G118 MOSFET and the HA2605(A1) and (A2) operational amplifiers. The HA2605(A3) operational amplifier, bias power supply subcircuit, and the circumvention subcircuit were replaced by equivalent impedances. For the bias power supply and circumvention subcircuits, these equivalent impedances consisted of single resistors. The HA2605(A3) operational amplifier was represented with a zener diode (orientation of the diode depended on the injected pulse polarity) for its input stage and by a 40-Ω resistor for its output resistance. The primary photocurrent generator contained in the zener diode model was used for simulating radiation effects.

4 RESULTS

The results for pulse entry point number one (Fig. 7) are shown in Table 3. By virtue of the nonlinearities of the components at the injected pulse levels used, the time signatures at their terminals nearly

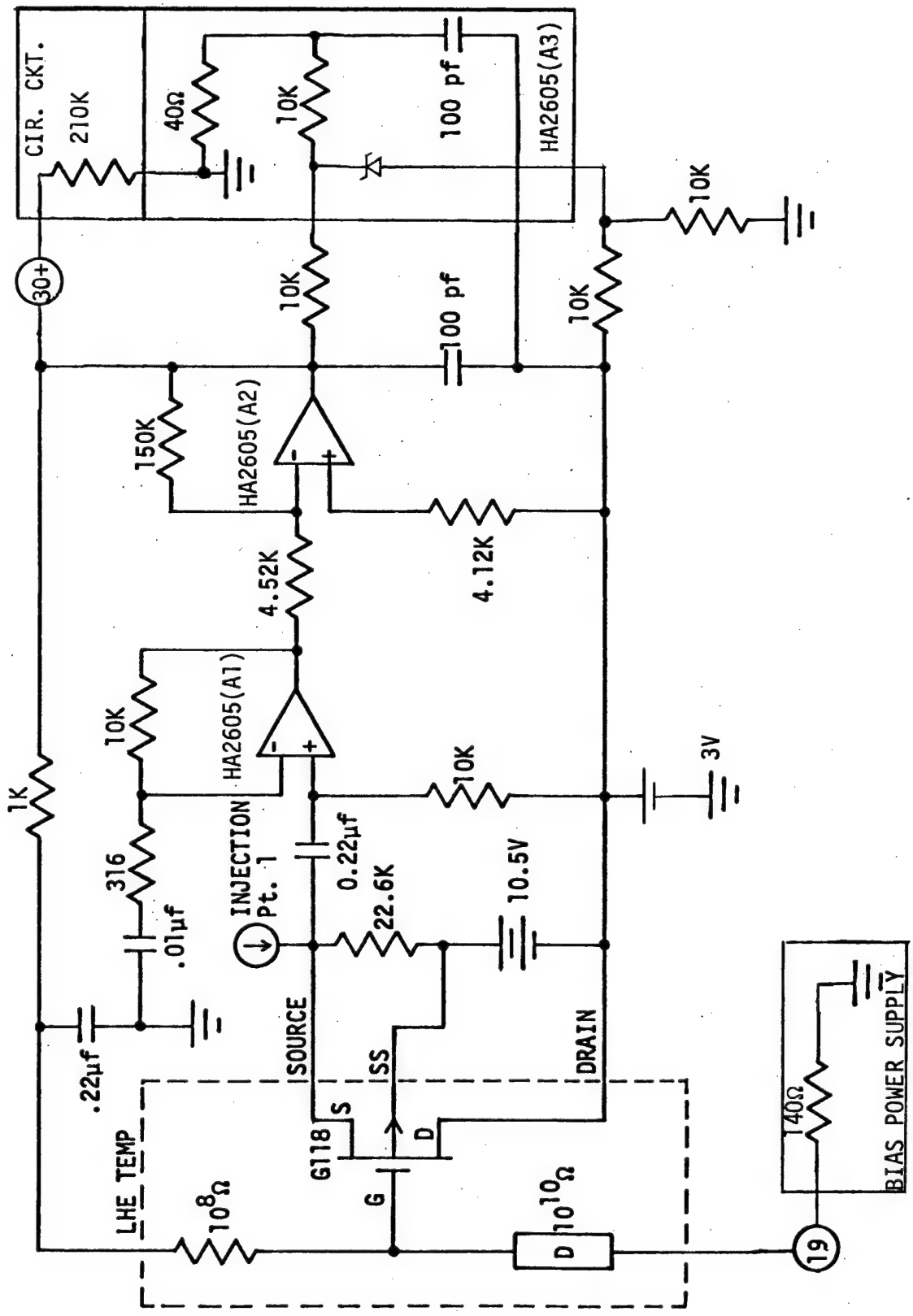


Figure 7. Circuit Model for Injection Point One

TABLE 3

RESULTS FOR PULSE ENTRY POINT 1

POINT 1			SUSCEPTIBLE DEVICE TERMINALS (V, A)		
Simulated Test	Polarity	Injected Pulse (V, A)	G118	HA2605(A1)	HA2605(A2)
EP[a]	+	(234., 5.5)	Gate (52., .6)	In^+ (225., 3.)[c]	In^+ (3.2, .003)
			Source (234., 2.1)	In^- (182., 0.45)	In^- (9.9, .001)
			Drain (3., 1.5)	Out (10.5, .01)	Out (-9.3, .013)
EP	-	(-140, 3.8)	Gate (-27., .4)	In^+ (-121., 3.2)[c]	In^+ (2.5, .002)
			Source (-140., .6)	In^- (-81., .2)	In^- (-10., .001)
			Drain (3., .2)	Out (-10., .01)	Out (9.5, .011)
CE[b]	+	(285., 10.)	Gate (72., 2.8)	In^+ (270, 5.96)[c]	In^+ (8.7, .002)
			Source (285., 3.4)[c]	In^- (220, .61)	In^- (6.5, .002)
			Drain (3.3, .56)	Out (11., .02)	Out (-9.4, .013)
CE	-	(-255., 8.2)	Gate (-38., 3.)	In^+ (-240., 5.)[c]	In^+ (2.8, .003)
			Source (-255., 3.15)[c]	In^- (-190., .4)	In^- (-2, .001)
			Drain (3., .15)	Out (-6, .03)	Out (8.8, .02)

a - EMP Simulated Environment
b - Combined TREE and EMP Simulated Environments
c - Location of Device Failure

always reached and maintained a constant value for most of the pulse duration. The results given for point one, and each of the other injection points, are the voltage and current values at the pulse midpoint, or at 0.5 μsec. The components judged susceptible to damage were the G118 MOSFET and the two HA2605 operational amplifiers, A1 and A2. Entry point one is the lead connecting the MOSFET source terminal to the A1 operational amplifier input. The A2 operational amplifier was also modeled so as to include the effects of the feedback loop from the output of A2 to the MOSFET gate. For the IEMP simulated test, the A1 operational amplifier is predicted to be the most vulnerable device. The critical injected pulse levels are 234 V, 5.5 A for a positive and -140 V, 3.8 A for a negative pulse. The predicted current path causing failure is from the positive differential input terminal to ground through a power supply terminal. For the combined effects case where a gamma radiation environment [10^{10} rad (Si)/sec] is included, both the G118 MOSFET and the A1 operational amplifier reach their failure levels as listed in Table 2. The critical injected pulse levels are 285 V, 10 A for a positive pulse and -255 V, 8.2 A for a negative pulse. The failure criteria (Table 2) for the HA2605 is for the terminal pair Out-In^+, where the pulse polarities were reversed to account for the predicted current pulse being in the opposite direction to the test condition. In general, for this and other components, failure was assumed if the signal at a component's terminal was within 10% or less of the corresponding value specified in Table 2. The failure criteria applied for the G118 was for the terminal pair G4-D as listed in Table 2. This data is available for positive pulses and IEMP effects only, but was applied to each simulation case due to the absence of other data. The main current path predicted to cause MOSFET failure is from the source terminal to the gate terminal, then through the gate protection diode to the substrate. The other failure criteria listed in Table 1 account for the fact that the G118 is manufactured with 6 gate terminals, 6 source terminals and 1 drain terminal. Since this analysis was for a 1-channel amplifier, however, only 1 gate and 1 source terminal were modeled. Nonetheless, the simulation results indicate that the gate voltage never reaches the failure level for the G1-G2 tests, and hence the G118 was predicted to not fail by this mode.

The analysis for pulse entry point two (Figs. 2 and 3) indicated that the DG143 was the only device susceptible to damage. Entry point two is the lead connected directly to the DG143 output terminals which are the drain connections for the two N-channel JFETs acting as switches within the device. One switch is normally open and one is normally closed. The failure data in Table 2 were obtained for the normally closed JFET switch. The results shown in Table 4 indicate failure occurs for an injected pulse of 225 V, 3.4 A for a positive pulse and -300 V, 4 A for a negative pulse. The current path in each case is from the JFET drain to source then through a biasing resistor (60 Ω in the worst case) to ground. Because failure data were lacking, and analysis including radiation effects was not performed.

TABLE 4

RESULTS FOR PULSE ENTRY POINT 2

POINT 2			SUSCEPTIBLE DEVICE TERMINALS (V, A)
Simulated Test	Polarity	Injected Pulse (V, A)	DG143
EP[a]	+	(255, 3.4)	Drain (255, 3.4)[b] Source (200, 3.4)
EP	-	(-300, 4)	Drain (300, 4)[b] Source (240, 4)

a - EMP Simulated Environment
b - Location of Device Failure

TABLE 5

RESULTS FOR PULSE ENTRY POINT 3

POINT 3			SUSCEPTIBLE DEVICE TERMINALS (V, A)
Simulated Test	Polarity	Injected Pulse (V, A)	DG143
EP[a]	+	(61., .064)	In^+ (61., .032)[b] In^- (3., .001)
EP	-	(-73, .39)	In^+ (-73., .35)[b] In^- (1.6, .001)

a - EMP Simulated Environment
b - Location of Device Failure

At pulse entry point number three (Fig. 3) the only device susceptible to damage is the DG143 differential input driver. Entry point three is the lead connected directly to the input terminal of the DG143. Table 5 gives the simulation results. In each case listed, the current pulse path causing damage is from the positive differential input terminal to the negative power supply terminal V_{EE}. The induced pulse predicted to cause damage is 61 V, 64 mA for a positive-biased pulse and -73 V, 0.39 A for a negative pulse. The damage criteria for the actively biased case were applied. A simulation including radiation effects was not performed for this injection point because of the lack of device radiation characteristics and failure criteria. On the basis of the results found for other injection points, however, an injected current pulse up to twice as large as for the IEMP-only case might be required to cause damage for the combined effects case.

The components deemed susceptible to damage due to pulse injection at entry point four were the two HA2605 operational amplifiers labeled A2 and A3 in Fig. 2 and the LM101 operational amplifier located nearest the pulse injection point as shown in Fig. 4. Table 6 indicates that failure in each case occurs at the output terminal of the HA2605(A3) operational amplifier. The main current path predicted to cause damage is from the output terminal to ground via a power supply terminal. The failure criteria applied from Table 2 are current values for the Out-In^+ terminal pair. For the combined effects case, a current pulse 1.7 to 2 times larger than for the IEMP environment only is required to cause damage.

The same components judged vulnerable for pulse entry point four were also used for the analysis of pulse entry point five, which is a lead connecting the preamplifier and the circumvention circuit. The results given in Table 7 indicate that the output terminal of the HA2605 (A2) operational amplifier is most vulnerable to damage. The main current path causing damage is from the output terminal to the power supply terminal of the IC device. The damage criteria applied were those given for Out-In^+ terminal pair. The results also indicate that again the device is up to twice as resistant to damage during the presence of gamma radiation.

Pulse entry point six is the sensor amplifier output terminal. Components vulnerable to an injected pulse at this point are the LM101 operational amplifier which acts as the final output stage of the logarithmic amplifier subcircuit of Fig. 6, and the two LM111 voltage comparators configured as Schmitt triggers in the threshold detector subcircuit, Fig. 5. To simplify the simulation only one LM111 was modeled. Current injection simulation results for point six are given in Table 8. The LM101 output terminal was found to be most susceptible to damage in each case. The current path causing damage was from the output terminal to ground through the device power supply terminal. The damage criteria applied were for the Out-In^+ terminal pair. Since

TABLE 6

RESULTS FOR PULSE ENTRY POINT 4

POINT 4			SUSCEPTIBLE DEVICE TERMINALS (V, A)		
Simulated Test	Polarity	Injected Pulse (V, A)	HA2605(A2)	HA2605(A3)	LM101
EP[a]	+	(558., 3.1)	In^+ (3., 10^{-4}) In^- (3., 10^{-4}) Out (.5, .009)	In^+ (9.2, .018) In^- (93., .009) Out (183., 3.)[c]	In^+ (12., 10^{-4}) In^- (34., 10^{-4}) Out (-9.8, 4mA)
EP	-	(-666., 3.1)	In^+ (3., 10^{-4}) In^- (3., 10^{-4}) Out (-.9, .019)	In^+ (-186., .037) In^- (-188., .01) Out (-280., 3.04)[c]	In^+ (-12, 10^{-4}) In^- (-34, 10^{-4}) Out (9.8, .005)
CE[b]	+	(900., 5.2)	In^+ (-2., .001) In^- (3.3, .001) Out (.7, .002)	In^+ (3., .024) In^- (6.3, .024) Out (250, 5.1)[c]	In^+ (147, .003) In^- (145, .003) Out (-10, .004)
CE	-	(-960., 6.1)	In^+ (2, .001) In^- (-3., .001) Out (-8., .02)	In^+ (-30., .03) In^- (-220., .015) Out (-310, 6.A)[c]	In^+ (-155, .01) In^- (-190., .03) Out (-13., .01)

a - EMP Simulated Environment
b - Combined TREE and EMP Simulated Environments
c - Location of Device

TABLE 7

RESULTS FOR PULSE ENTRY POINT 5

POINT 5			SUSCEPTIBLE DEVICE TERMINALS (V, A)		
Simulated Test	Polarity	Injected Pulse (V, A)	HA2605(A2)	HA2605(A3)	LM101
EP[a]	+	(550., 3.2)	In^+ (3., 10^{-4}) In^- (4.7, 10^{-4}) Out (151., 3.03)[c]	In^+ (3., 10^{-4}) In^- (24., .009) Out (-9.6, .004)	In^+ (54., .004) In^- (24., 10^{-4}) Out (10.1 .002)
EP	-	(-522., 3.2)	In^+ (3., 10^{-4}) In^- (6., 10^{-4}) Out (-122. 3.06)[c]	In^+ (3., 10^{-4}) In^- (-24, .006) Out (9.6, .004)	In^+ (-181., .001) In^- (-121., .001) Out (-10., .007)
CE[b]	+	(848., 5.2)	In^+ (10^{-3}, .019) In^- (-2.1, .02) Out (199., 4.97)[c]	In^+ (10^{-4}, .019) In^- (-1.5, .019) Out (-9.8, .003)	In^+ (254., .003) In^- (192., .003) Out (10., 10^{-4})
CE	-	(-995., 6.1)	In^+ (10^{-3}, .02) In^- (-90., .019) Out (-233., 5.84)[c]	In^+ (10^{-4}, .02) In^- (-26., .02) Out (10., .005)	In^+ (-693., .01) In^- (-695., .01) Out (-10., .005)

a - EMP Simulated Environment
b - Combined TREE and EMP Simulated Environments
c - Location of Device Failure

TABLE 8

RESULTS FOR PULSE ENTRY POINT 6

Point 6			SUSCEPTIBLE DEVICE TERMINALS (V, A)	
Simulated Test	Polarity	Injected Pulse (V, A)	LM101	LM111
EP[a]	+	(205., 5.4)	In^+ (.1, 10^{-4}) In$^-$ (15., .03) Out (205., 4.8)[c]	In^+ (126., .001) In$^-$ (205., .6) Out (-9.6, .007)
EP	-	(-190., 5.)	In^+ (-.12, 10^{-4}) In$^-$ (-16., 10^{-5}) Out (-190., 4.4)[c]	In^+ (-113., 10^{-4}) In$^-$ (190., .54) Out (9.8, .005)
CE[b]	+	(195., 5.4)	In^+ (.15, .002) In$^-$ (14., .001) Out (195., 4.6)[c]	In^+ (172., 10^{-4}) In$^-$ (195., .82) Out (-22., .018)
CE	-	(-190., 5)	In^+ (.1, .001) In$^-$ (13.6, .002) Out (-190., 4.4)[c]	In^+ (-112., 10^{-4}) In$^-$ (-190., .54) Out (-2.2, .005)

a - EMP Simulated Environment
b - Combined TREE and EMP Simulated Environments
c - Location of Device Failure

no damage criteria were availabe for the LM111, criteria for similar device types (i.e., LM101 and LM108) were used. The results indicate that the presence of a gamma environment had little effect on the damage vulnerability for this injection point. The output of the LM111 does not reach the damage level indicated for the SN54L00 TTL gate. However, information regarding the nonlinear operation of a TTL gate obtained from HDL during the performance of this contract indicates that the higher than normal output voltage of the LM111 during the pulse injection will probably cause the SN54L00 to change logic states.

In summary: the results indicate that the circuit is most vulnerable to a pulse induced at entry point three, the lead between the bias power supply and the bias control switch (see Fig. 3). For this point the vulnerable component is the DG143 differential input driver composing part of the bias power supply circuitry. The critical induced pulse level found for the IEMP environment for the circuit was 61 V, 0.064 A for a positive-biased pulse, and -73 V, 0.39 A for a negative-biased pulse. With the inclusion of radiation effects, the critical pulse level required for circuit failure is estimated to be a factor of 2 larger. The next most vulnerable circuit locations were for pulses injected at entry points one, four, and five. These points were all found to have approximately equal vulnerability, with damage occurring for 3-A pulses. The vulnerable component in each case was one of the HA2605 operational amplifiers (depending on the particular pulse entry point) located in the preamplifier subcircuit.

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1	Teledyne Brown Engineering Company ATTN: Mr. G. R. Ezell Research Park 300 Sparkman Drive Huntsville, Alabama 35807	1
	Vought Missiles & Space Company ATTN: Mr. William McMillin P. O. Box 6267 Dallas, Texas 75222	1
	TOTAL	72